**Abstract:** A four level static compensator integrating two 2 level converters, supplying/absorbing reactive power to/from the grid, is reported in our earlier paper. Reduced component count, simpler layout for switches, and smaller DC link capacitor values are the attractive features of the proposed topology over the diode clamped and cascaded multilevel converters. This paper suggests asymmetric twin converter topology. Suitable selection of the DC link voltage values reduces distortion in the current fed to the grid. In addition, circuit topology is modified to avoid the split-capacitor DC links. This reduces the number of independent DC capacitor voltages to be controlled and eliminates the flow of third harmonic current through the transformer. In order to improve the performance, a phase shifted carrier-based pulse width modulation technique is used. A mathematical model of the system is derived, based on which a controller for the scheme is designed. The effectiveness of the scheme is verified through detailed simulation study. This paper implements with the advanced concept is Fuzzy logic. In this method of rule based decision making used for expert systems and process control that emulates the rule of thumb thought process used by human beings. Fuzzy logic arose from the DC voltage control and reduces the total harmonic distortion.

**Keywords:** Carrier Based Pulse Width Modulation (CBPWM), Pulse Width Modulation (PWM), Static Synchronous Compensator (STATCOM), Total Harmonic Distortion (THD).
1. Introduction:

To provide transmission line voltage support, a Static Synchronous Compensator (STATCOM) offers the optimal solution in terms of price, reliability and dynamic performance [2], [3]. Generally, multipulse converter based [4] and multilevel converter based [5]–[8] solutions are used for high power applications. A multipulse converter uses more than one voltage source converter (VSC), with common DC link, operating with nearly fundamental switching frequency and the output of each module is connected in series through the multipulse transformer. By adjusting the triggering pulses of different VSCs, specified Total Harmonic Distortion (THD) of the injected current is achieved with reduced switching losses as compared to that of single VSC based solution. The major drawback of this scheme is the high cost and complex structure of the bulky multipulse transformer. The second solution is multilevel converters [5]–[8], which provide more than two steps in the voltages, thereby reducing THD without switching semiconductor devices at a high frequency. The two most commonly used schemes are diode clamped and cascaded converter topologies. The diode clamped multilevel topology is mostly restricted to a three level configuration because of the complex layout of the diodes (which grows as the square of the number of levels) and the need for capacitor voltage balancing [5].

The other commonly used multilevel topology, i.e. cascaded converter topology [9]–[13], comprises several single phase H bridge/full bridg converters, with separate dc links. The following are the two associated problems of this topology:

   i. The size of the DC-link capacitor required is high because the instantaneous power involved with each module varies at twice the fundamental frequency [14] and
   ii. The regulating voltage across a large number of self-supported dc-link capacitors makes the controller design complex [12], [15]–[23].

To address some of the aforementioned limitations in multilevel converters, a four level asymmetric twin converter topology based multilevel converter, shown in Fig. 1, is proposed in [28]. This topology uses a reduced number of components (12 controlled switches with antiparallel diodes) as compared to the diode clamped topology (18 controlled switches with antiparallel diodes plus 18 diodes) [5]. Moreover, in this case, semiconductor switches are arranged as VSC, which enables easier structural layout and reduced driver circuit complexity. Therefore, standard VSC power modules [include six Insulated Gate Bipolar Transistors (IGBTs) and their driver circuits in one package] can be used instead of discrete
components. Moreover, this topology utilizes cascade connection of three phase VSCs, and hence, the size of the DC link capacitor is less as compared to that in cascaded H-bridge multilevel converter. The reduced number of DC links makes voltage regulation easier as compared to that in an equivalent cascaded converter. Comparison of diode clamped converter, cascaded converter, and open ended transformer topologies for various parameters is given in [1].

STATCOM (Static Synchronous Compensator), which is consists of a two level Voltage Source Converter (VSC), a DC energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the DC voltage across the storage device into a set of three phase AC output voltages. These voltages are in phase and coupled with the AC system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the STATCOM output voltages allows effective control of active and reactive power exchanges between the STATCOM and the AC system. Such configuration allows the device to absorb or generate controllable active and reactive power. But, there are several factors that must be considered when designing the STATCOM and associated control circuits.

2. Proposed Methodology:

The asymmetric twin converter topology is proposed in this paper wherein only two DC links are used without split capacitor arrangement, as shown in Fig. 1. Furthermore, the THD of currents supplied to the grid is reduced by selecting a suitable ratio of DC link voltages of the two VSCs. A ratio of 1:0.366 is selected based on the study of open ended induction motor drive, which has similar power circuit configuration [25].
Figure 1: Asymmetric twin converter topology based STATCOM

In this paper, the principle of operation of the proposed scheme and a suitable pulse width modulation (PWM) technique. Various switching states and corresponding phase voltages are provided to justify the four level operation of the circuit. A mathematical model of the proposed topology is describes the development of the controller. Operation of DC voltage regulator and reactive power controller are also discussed.

A. Principle of Operation:

The proposed asymmetric-twin-converter-based multilevel topology, comprising two VSCs, is shown in Fig. 1. Low voltage (LV) windings of the transformer are connected differentially between two 2 level VSCs such that the voltage appearing on the LV side is the difference of the output voltages of two VSCs. High-voltage (HV) windings, arranged in a star configuration, are connected to the three-phase grid. Leakage inductances of the transformers act as input filter inductances of the STATCOM. Both VSCs operate with separate DC links to produce two level individual output. Voltages appearing on the LV windings of the transformer are written in terms of output voltages of VSCs as

\[ \begin{align*}
    e_a &= e_{a1g1} - e_{a2g2} + e_{g1g2} \\
    e_b &= e_{b1g1} - e_{b2g2} + e_{g1g2} \\
    e_c &= e_{c1g1} - e_{c2g2} + e_{g1g2}. \\
\end{align*} \tag{1} \]

where \( e_a, e_{a1g1}, e_{a2g2}, \) and \( e_{g1g2} \) are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative DC link terminals of the two VSCs, respectively. Since both VSCs have separate DC links, the sum of the LV winding phase currents should be zero

\[ i_a + i_b + i_c = 0 \tag{2} \]
Furthermore, the sum of instantaneous values of grid voltages is equal to zero
\[ V_a + V_b + V_c = 0. \]  \hspace{1cm} (3)

The sum of the LV winding voltages is given by
\[ e_a + e_b + e_c = \frac{N_{LV}}{N_{HV}}(v_a + v_b + v_c) - r(i_a + i_b + i_c) - L \frac{d(i_a + i_b + i_c)}{dt} \]  \hspace{1cm} (4)

where \( r \) and \( L \) are the resistance and leakage inductance as measured from the LV side, respectively, and \( N_{LV}/N_{HV} \) is the turns ratio. Substituting (2) and (3) into (4) gives
\[ e_a + e_b + e_c = 0. \]  \hspace{1cm} (5)

Substituting LV voltages from (1) in (5) results in
\[ e_{g1g2} = \frac{1}{3}(e_{a1g1} - e_{a2g2}) - \frac{1}{3}(e_{b1g1} - e_{b2g2}) - \frac{1}{3}(e_{c1g1} - e_{c2g2}) \]  \hspace{1cm} (6)

Substituting the value of \( e_{g1g2} \) in (1) yields
\[ \begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} e_{a1g1} - e_{a2g2} \\ e_{b1g1} - e_{b2g2} \\ e_{c1g1} - e_{c2g2} \end{pmatrix} \]  \hspace{1cm} (7)

The line voltages of the LV side \( e_{ab}, e_{bc} \) and \( e_{ca} \) are expressed as pole voltages using (1)
\[ \begin{align*}
e_{ab} &= e_a - e_b = e_{a1g1} - e_{a2g2} - e_{b1g1} + e_{b2g2} \\
e_{bc} &= e_b - e_c = e_{b1g1} - e_{b2g2} - e_{c1g1} + e_{c2g2} \\
e_{ca} &= e_c - e_a = e_{c1g1} - e_{c2g2} - e_{a1g1} + e_{a2g2}
\end{align*} \hspace{1cm} (8)

For \( V_{dc2} = 0.5V_{dc1} \), depending on the state of switches, voltage waveforms of \( e_{ab}, e_{bc} \) and \( e_{ca} \) has seven different steps.

**B. PWM Strategy:**

Hence, the use of phase-shifted (PS) CB-PWM is suggested for the proposed topology. This PWM technique expects the controller to generate individual modulating waveforms for each inverter output \( e_{ag1}, e_{bg1}, e_{cg1}, e_{a2g2}, e_{b2g2} \) and \( e_{c2g2} \).
Each modulating waveform is compared with a carrier waveform to determine the switching state of the corresponding inverter devices. This is similar to the PS CB-PWM technique used in H-bridge cascaded converters [26], [27]. For two H-bridges per phase, the resultant waveform of AC voltages is the sum of individual converter voltages. Therefore, carrier waveforms are 180° PS from each other to cancel the carrier frequency harmonics. However, in the case of asymmetric twin converter topology, the shift in carriers is not required because the resultant waveform is the difference of two AC voltages. Comparison of modulating and carrier signals for phase-a. Modulated converter voltages \( e_{a1g1}, e_{a2g2} \) and \( e_a \) for the simulated case of \( V_{dc1} = 805 \) V, \( V_{dc2} = 294 \) V, fundamental frequency \( f = 50 \) Hz, carrier frequency \( f_c = 900 \) Hz, and modulation index \( m = 0.9 \) are shown in Fig. 2.

3. Development Of The Equivalent Circuit:

For the purpose of analysis, an equivalent circuit of the proposed STATCOM is derived and is shown in Fig. 3. Transformer is represented by equivalent series combination of inductances, resistances, and voltage sources. To model the losses in two VSCs, two resistances \( r1 \) and \( r2 \) are placed in parallel to the two DC links.

The governing equations of the proposed system can be derived as
where $L$ is defined as $\omega_b l / z_{base}$. $\omega_b$ and $z_{base}$ are the leakage inductance, base frequency and base impedance of STATCOM. All the parameters and variables are expressed in per unit (p.u.) system. Equation (9) is transformed into dq0 reference frame. The system variables in the dq0 frame are expressed as follows

$$S = \begin{bmatrix} -\frac{\omega_b}{L} & 0 & 0 \\ 0 & -\frac{\omega_b}{L} & 0 \\ 0 & 0 & -\frac{\omega_b}{L} \end{bmatrix}$$

$$i_0 = \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}, \quad \omega_b \begin{bmatrix} e_d + V_c \\ e_q + V_c \\ -e_d - e_q + V_l \end{bmatrix}$$

Equation (10) interrelates the AC parameters of the STATCOM with those of the grid. The dependence between DC and AC parameters of STATCOM is derived using instantaneous power balance equations. The following equation gives the power balance condition between the AC and DC links of VSC-1

$$V_{dc1} i_{dc1} = \frac{3}{2} \left( e_{d1} i_d + e_{q1} i_q \right)$$

The current flowing through the DC link capacitor $C_1$ is related to the DC link voltage $V_{dc1}$ as follows

$$SV_{dc1} = \omega_b C_1 \left( i_{dc1} - V_{dc1} \right)$$

where $C_1$ is defined as $1/(\omega_b C_1 z_{base})$. Substituting $i_{dc1}$ from equation (11)

$$SV_{dc1} = \omega_b C_1 \left( \frac{3}{2V_{dc1}} (e_{d1} i_d + e_{q1} i_q) - \frac{V_{dc1}}{r_1} \right)$$

Similarly, the governing equation for VSC-2 is expressed as

$$SV_{dc2} = \omega_b C_2 \left( \frac{-3}{2V_{dc2}} (e_{d2} i_d + e_{q2} i_q) - \frac{V_{dc2}}{r_2} \right)$$
Equations (10), (13), and (14) represent the behavior of the system.

4. Development of Controller:

The proposed asymmetric twin converter based STATCOM has two DC link voltages $V_{dc1}$ and $V_{dc2}$. The controller should regulate these two DC link voltages and govern the total reactive power flowing to/from the STATCOM. The total active power required to overcome losses and regulate DC link voltages is drawn by STATCOM from the grid. This active power needs to be redistributed among the two DC links. The distribution should ensure that the two DC link voltages $V_{dc1}$ and $V_{dc2}$ are maintained equal to their corresponding reference values.

![Controller for STATCOM](image)

Figure 4: Controller for STATCOM

5. Current Control:

The overall system is represented by two coupled differential equations, as depicted in (10). To decouple them, two variables $x1$ and $x2$ are defined such that

$$-e_{d1} + e_{d2} = \frac{L}{\omega_b} (x_1 - \omega i_d) - |V|$$  \hspace{1cm} (15)

$$-e_{q1} + e_{q2} = \frac{L}{\omega_b} (x_2 + \omega i_d)$$  \hspace{1cm} (16)

By combining (10) with (15) and (16), the decoupled system equations are obtained as follows:

$$S\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \end{pmatrix} = \begin{pmatrix} -\frac{\omega_0}{\omega_b} & 0 \\ 0 & \frac{\omega_0}{\omega_b} \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix} + \begin{pmatrix} \omega_b \\ \frac{\omega_0}{L} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix}$$  \hspace{1cm} (17)
Applying small signal analysis on the decoupled system of (17), the small signal plant transfer function is derived as

$$G(S) = \frac{\Delta i_s}{\Delta x_1} = \frac{1}{S + \frac{R_0}{L}}$$  \hspace{1cm} (18)$$

Control variables \(x_1\) and \(x_2\) govern the system currents \(i_d\) and \(i_q\), respectively, as per the differential equation (17). Therefore, current control is achieved by controlling variables \(x_1\) and \(x_2\) using the errors between reference values and actual currents, as given by

$$X_1 = k_p (i_{d,ref} - i_d) + k_d \int (i_{d,ref} - i_d) dt \hspace{1cm} (19)$$

$$X_2 = k_p (i_{q,ref} - i_q) + k_d \int (i_{q,ref} - i_q) dt \hspace{1cm} (20)$$

Required LV voltages \(e_{d1} - e_{d2}\) and \(e_{q1} - e_{q2}\) are derived by using these values of \(x_1\) and \(x_2\) in (15) and (16). To generate these voltages, modulation signals for the VSCs are derived as follows

$$m_{d1} = \frac{e_{d1}}{V_{dc1}}; \quad m_{d2} = \frac{e_{d2}}{V_{dc2}}; \quad m_{q1} = \frac{e_{q1}}{V_{dc1}}; \quad m_{q2} = \frac{e_{q2}}{V_{dc2}}; \hspace{1cm} (21)$$

An inner current controller is implemented using (15), (16), and (19)–(21), as shown in Fig. 4.

**B. Reactive Power Control:**

STATCOMs are commonly used either for transmission line voltage support or for reactive power compensation of load. For voltage support of the transmission line, the reactive current reference \(i_{q,ref}\) is controlled by the deviation of the transmission line voltage from its nominal value. On the other hand, for load compensation operation, the reactive current reference \(i_{q,ref}\) is controlled by the deviation of source power factor from its required value. In both the aforementioned cases, \(i_{q,ref}\) will be supplied to the current controller by a higher level controller.

**C. DC Voltage Control:**

i. **Sum of DC Voltages:** The sum of the dc voltages \((V_{dc1} + V_{dc2})\) increases with the net real power flow from grid to STATCOM and vice versa. In other words, the error in the sum of DC link voltages \((V_{dc1} + V_{dc2} - V_{dc1-ref} - V_{dc2-ref})\) indicates the amount of real power to be absorbed from the grid. Hence, the d-axis reference current \(i_{d,ref}\) is
controlled by the error existing between reference and actual DC link voltages of VSCs, as shown in Fig. 4.

ii. Difference of DC Voltages: System equations (13) and (14) are coupled equations describing the behavior of the DC link voltages. Considering \( C_1 = C_2 = C \) and subtracting (14) from (13) give

\[
S(V_{dc1} - V_{dc2}) = X_3 - \alpha_0 C \left( \frac{V_{dc1}}{r_1} - \frac{V_{dc2}}{r_2} \right)
\]

\[
X_3 = \frac{3\alpha_0 C}{2} \left[ i_d \left( \frac{e_{d1}}{V_{a1}} + \frac{e_{d2}}{V_{a2}} \right) + i_q \left( \frac{e_{q1}}{V_{a1}} + \frac{e_{q2}}{V_{a2}} \right) \right]
\]

iii. Substituting modulation signals from (21) into (23) gives

\[
X_3 = \frac{3\alpha_0 C}{2} \left[ i_d (m_{d1} + m_{d2}) + i_q (m_{q1} + m_{q2}) \right]
\]

\[
X_3 = \frac{3\alpha_0 C}{2} (\bar{m} \ast \bar{i})
\]

where the modulation vector \( \bar{m} = m_{d1} + m_{d2} + j(m_{q1} + m_{q2}) \) and the current vector \( \bar{i} = i_d + j i_q \).

Considering \( r_1 = r_2 = r \) and applying small signal analysis on (22) give the transfer function

\[
H(S) = \frac{\Delta V_{dc1} - \Delta V_{dc2}}{\Delta X_3} = \frac{1}{S + \frac{\alpha_0 C}{r}}
\]

Hence, the difference in power requirement between VSC-1 and VSC 2 is reflected in \( X_3 \).

Using it, \((\bar{m} \ast \bar{i})\) is determined from (25). To achieve the required power flow between VSCs with low DC link voltages, the modulation vector \( \bar{m} \) is maintained in phase with \( \bar{i} \). Hence

\[
|\bar{m}| = \frac{2}{3\alpha_0 C |\bar{i}|} X_3, \quad \angle \Delta \bar{m} = \bar{i}
\]

The controller which ensures that the difference of DC voltages \( V_{dc1} - V_{dc2} \) is maintained equal to the reference \( V_{dc1_{ref}} - V_{dc2_{ref}} \) is shown in Fig. 4.

\[\text{D. Generation of Modulation Signals:}\]

The current controller, shown in Fig. 4, generates the signals for primary voltages \( e_{d1} - e_{d2} \) and \( e_{q1} - e_{q2} \). These are transformed to modulation signals as follows:

\[
m_{d1} V_{a1} - m_{d2} V_{a2} = e_{d1} - e_{d2}
\]

\[
m_{q1} V_{a1} - m_{q2} V_{a2} = e_{q1} - e_{q2}
\]
Furthermore, the “Difference of DC Voltages” controller generates $m_{d1} + m_{d2}$ and $m_{q1} + m_{q2}$. By arithmetic operation on the outputs of these two controllers, the individual modulation signals for the two VSCs $m_{d1}$, $m_{q1}$, $m_{d2}$, and $m_{q2}$ are generated by the block “Modulation Signals Generator,” as shown in Fig. 4. These signals are then converted to stationary abc frame of reference. The modulation waveforms for the two VSCs are then compared with the carrier waveforms to generate gating signals for VSCs.

The simulation circuit for asymmetric twin converter STATCOM is shown in Fig. 5. The distribution should ensure that the two DC link voltages $V_{dc1}$ and $V_{dc2}$ are maintained equal to their corresponding reference values as show in fig. 5.

![Figure 5: Simulation Circuit for Asymmetric Twin Converter Topology Based High Power STATCOM](image)

The simulation circuit on controller for STATCOM is shown in Fig. 6.

![Figure 6: Simulation Circuit on Controller for STATCOM](image)
6. Results:

The results of the simulation files of Asymmetric Twin Converter Based STATCOM and Fuzzy Logic based STATCOM are shown below.
Figure 9: Simulated Transient Test Results. (i) LV-side voltage $e_a$. (ii) LV-side phase-a transformer current $i_a$. (iii) p.u. reactive current $i_q$. (iv) DC link voltages $V_{dc1}$ and $V_{dc2}$.

Figure 10: Total Harmonic Distortion of LV Side Voltage ($e_a$) For Asymmetric Twin Converter Based STATCOM

Figure 11: Total Harmonic Distortion of LV-Side Voltage ($e_a$) For Fuzzy Logic Based STATCOM
7. Conclusion:

A high-power STATCOM based on two 2-level VSCs is reported in [1]. Reduced component count, simpler layout of switches and reduced capacitance requirement are the attractive features of the scheme over the diode clamped and cascaded multilevel converters. In the proposed topology, only two DC voltages have to be controlled. Furthermore, the ratio of the DC link voltages of the two VSCs is selected such that low distortion in current is achieved. A DC link voltage controller has been proposed to regulate the DC link voltages of the two converters by drawing requisite amount of real power from the utility and by differentially distributing them between the two converters. A mathematical model of the system is developed to facilitate the design of the controller. Simulation results carried in a simulation study of proposed topology has been carried out using MATLAB/Simulink and the results are presented.
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