Abstract: Integrated Circuits (ICs) have grown in size and complexity as per Moore’s law. By scaling down a feature size increases probability of defects during manufacturing process. Testing required to guarantee fault-free products. In this, we can design a testable circuit in reversible manner. Reversible logic is one of the upcoming low power logic in VLSI. Reversible circuits are those circuits that do not lose information during computation and reversible computation in a system can be performed only when the system comprises of reversible gates. In this paper, we implement reversible universal shift register which can be testable for both stuck at fault. The proposed universal shift register is a register that has both shifts and parallel load capabilities and with the help of reversible gates we can achieve testing capability.

Keywords: Reversible logic, testable circuit, universal shift register.
1. Introduction:

Space and mobile applications demand performance, low power dissipation, and fault tolerance. The major limitation in this type of applications is that the hardware executing the same has to survive on battery/solar power. Hence, these systems are to be extremely power aware. Traditional fault-tolerant systems that use techniques such as triple-modular redundancy (TMR) consume more logic and, hence, dissipate larger power than non fault-tolerant versions of the same. As a result, the overall power dissipation of the chip significantly increases. This, in turn makes the system power hungry and, hence, not suitable for portable applications. Another major application of hardware that is well reported in the literature is in the real-time/online safety critical system domain. For example, the safety logic systems for nuclear reactors are essentially hardware based and are greatly exposed to charged particles. Specifications of such systems demand online detection of faults to ensure correct and safe execution.

Among the emerging computing paradigms, reversible logic appears to be promising due to its wide applications in emerging technologies. Some of the emerging nanotechnologies having applications of reversible logic are quantum computing, quantum dot cellular automata (QCA), optical computing, Spintronics, DNA computing, molecular computing and also in power-efficient nanocomputing. Landauer has shown that during irreversible computation 1 bit of information lost results in KTB Joules of energy dissipation [1]. Bennett in another seminal contribution proved that this KTB joules of energy dissipation will not occur if computation is performed in a reversible manner [2].

Conservative logic is a logic family that exhibits the property that there are an equal number of 1s in the outputs as there are in the inputs [3]. Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one to-one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa. Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there are equal number of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible [4], if one-to-one mapping between the inputs and the outputs vectors is not preserved.
In existing literature, they have proposed a design of testable reversible D latch using conservative Fredkin gate. In this paper, we proposed a new approach for designing universal shift register which performs parallel loading as well as shift operations like left/right.

2. Basic Reversible Gates:

Several reversible gates such as the Peres gate [5], the Fredkin gate, the Toffoli [6] gate and the TR gate exists in the literature. The quantum cost of reversible gate is the number of 1x1 and 2x2 reversible gates needed to design a 3x3 reversible gate.

2.1. NOT Gate:

A NOT gate is 1x1 gate represented as shown in Fig. 1. Since it is a 1x1 gate, its quantum cost is unity.

The quantum cost of NOT Gate is 1.

\[ A \xrightarrow{\oplus} P = \overline{A} \]

*Figure 1: NOT Gate*

2.2. Feynman Gate:

The Feynman gate (FG) or the controlled-NOT gate (CNOT) is a 2-input and 2-output reversible gate with the mapping \((A, B)\) to \((P=A, Q=A \oplus B)\) as shown fig 2. Here A is the controlling input and B is the controlled input; P, Q are the two outputs. It has a quantum cost of 1. Feynman gate can be used for copying/complementing \((A=0/1)\) the signal. The quantum cost of Feynman Gate is 1.

\[ A \xrightarrow{} P = A \\
B \xrightarrow{} Q = A \oplus B \]

*Figure 2: Feynman Gate*
2.3. Fredkin Gate:

Fredkin gate is a 3x3 reversible logic gate with three inputs and three outputs as shown in Fig 3. The Fredkin gate maps (A, B, C) to (P=A, Q=A’B+AC, R=AB+A’C), where A, B, C are the inputs and P, Q, R are the outputs, respectively [18]. A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. The quantum cost of Fredkin Gate is 5.

2.4. Peres Gate:

The Peres gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A ⊕ B, R= A·B ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fig 4 shows representation of Peres gate. The quantum cost of Peres Gate is 4.

2.5. Toffli Gate:

The Toffli gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q= B, R= A·B ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fig 5 shows representation of Toffli gate.
The Toffoli Gate (TG) is a 3x3 two-through reversible gate as shown in Fig.5. Two through means two of its outputs are the same as the inputs with the mapping (A, B, C) to (P=A, Q=B, R=A•B⊕C), where A, B, C are inputs and P, Q, R are outputs, respectively. Fig 5 shows toffli gate representation. The quantum cost of Toffli Gate is 5.

3. Universal Shift Register:

The Universal shift register is a register that has both shifts and parallel load capabilities. The reversible universal shift register needs to have the following functionalities and components:

i. Testable Reversible D flip-flops.
ii. Testable Parallel-Load Circuit.
iii. Feyman Gate

3.1. Building Blocks For Shift Register:

This section presents design of reversible D flip flop and parallel loading components in testable shift register.

3.1.1. Testable Reversible D Flip-Flop:

The design of the Reversible D flip flop [7] is shown in Figure 6. The design has 1 Fredkin gates and 1 Peres gate. We can observe that the first Fredkin gate maps the D flip flop characteristic equation. The characteristic equation of D flip flop is while the second Fredkin gate has two control inputs C1 and C2. When C1=0 and C2=1, the design works in normal mode implementing the D latch characteristic equation[8].

In test mode, when C1C2 = 00 it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected.

When C1C2 = 11, the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault.

\[ Qi^+ = \overline{CLK} \ Q + CLK \ D \]
3.1.2. Testable Parallel Loading Circuit:

Parallel loading of reversible shift registers is another step in the evolution of shift registers. The circuit can load $X$ bits ($X$ is an input vector consisting of $n$ bits: $X_{n-1} X_{n-2} X_{n-3} \ldots X_2 X_1 X_0$) directly into the flip-flops, the same as a buffer register. This kind of entry is called parallel or broadside loading; it takes only one clock pulse to store an entire digital word.

\[
Q_{i}^+ = \text{SHL} \cdot Q_{i-1} \oplus \text{LOAD} \cdot X \oplus \overline{\text{LOAD}} \cdot \text{SHL} \cdot Q_i
\]

The input of the testable shift register is:

i. LOAD, SHL: control signals of shift register

ii. $X_i$: $i^{th}$ data input to the shift register

iii. $Q_{i-1}, Q_i$: output of the $(i-1)^{th}$ and $i^{th}$ D Flip Flop.
iv. C1,C2: control input for test mode.

The output of the testable shift register is:

\[ Q_i^+ \text{, LOAD, SHL, } Q_i \] It would be regenerated to drive next bit position’s parallel loading circuit.

### 4. Proposed Testable System:

The working of the testable reversible universal shift register [9] can be described as follows. The truth table for the operation of shift register as shown in Table 1

<table>
<thead>
<tr>
<th>LOAD</th>
<th>SHL</th>
<th>FINAL OUTPUT (Q_i^+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q_i (No Change)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Q_{i-1} (left shift)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X_i (LOAD from vector X)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>*(Forbidden)</td>
</tr>
</tbody>
</table>

*Table 1: The truth table for the operation of shift register*

*Figure 8: proposed testable universal shift register*
i. When LOAD SHL: 00, the outputs of each Proposed D flip-flops are fed back as inputs to them. Thus during the next edge of the clock, the same value is maintained at the outputs of the reversible flip flops and no change occurs in their states.

ii. When LOAD SHL =01, D_in is selected and loaded into the flip flop. The parallel loading circuit act the exact same way for their corresponding flip flops.

iii. When LOAD SHL =10, there is a transfer of information from parallel input lines to the reversible D flip flops, simultaneously, in the next clock edge.

iv. When LOAD SHL=11, it will be in forbidden state.

4.1. Modes Of Operation:

There are two modes in proposed design. The control inputs are used to select mode of operation.

4.1.1. Normal Mode:

When C1=0 and C2=1, the design will be in normal mode. It will act as universal shift register.

4.1.2. Test Mode:

4.1.2.1. Stuck At 1 Fault:

When C1C2 = 00, it will make the design testable with all 0s input vectors as output S1&S2 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected.

4.1.2.2. Stuck At 0 Fault:

When C1C2 = 11, the output S1&S2 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault[10].

Hence the proposed shift register is testable for both stuck at faults. We can detect these faults with help of control inputs.
5. Results And Discussion:

5.1. Evaluation Of Proposed Testable Reversible Shift Register:

5.1.1. Quantum Cost:

The quantum cost of a reversible gate is the number of reversible or quantum logic gates required in its design.

5.1.2. Delay:

The delay is the maximum number of gates in a path from any input line to any output line.

5.1.3. Garbage Outputs:

Unwanted or unused outputs which are needed to maintain reversibility of a reversible gate (or circuit) are known as Garbage Outputs.

The proposed Reversible Universal Shift Register has quantum cost of 140, delay 140 and 35 garbage bits. The proposed design of Reversible Universal Shift Register achieves improvement ratios of 21% in terms of quantum cost, delay and garbage outputs compared to the design presented in existing [12]. The improvement ratios compared to the design presented in existing [12] in terms quantum cost and delay. The results are summarized in Table 2.

<table>
<thead>
<tr>
<th>Design of Reversible Shift Register</th>
<th>Quantum Cost</th>
<th>Delay</th>
<th>Garbage Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>144</td>
<td>144</td>
<td>35</td>
</tr>
<tr>
<td>Existing[12]</td>
<td>220</td>
<td>220</td>
<td>36</td>
</tr>
<tr>
<td>Improvement in % w.r.t[12]</td>
<td>21</td>
<td>21</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table 2: Comparison of Reversible Shift Register

5.2. Simulation Results:

The Proposed universal shift register is simulated using Xilinx ISE software. Fig 9 shows simulation of proposed testable reversible DFF.
Figure 9: proposed testable reversible DFF

Fig. 10 represents a simulation of testable parallel loading circuit. Fig. 11 represents a technological view of proposed testable universal shift register.

Figure 10: simulation of testable parallel loading circuit

Figure 11: Technological view of Proposed Testable Universal Shift Register
6. **Application:**

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance. It includes the area like

i. Low power CMOS.

ii. Quantum computer.

iii. QCA Devices[11]

iv. Nanotechnology

v. Optical computing

vi. Design of low power arithmetic and data path for digital signal processing (DSP).

vii. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

7. **Conclusion:**

This paper presents design of universal shift register which can be testable for both stuck at faults. The proposed design have the applications in building reversible ALU, reversible processor etc. Further, we have demonstrated a methodology of error detection in reversible logic circuits. The proposed methodology of error detection based on property of reversible logic is generic in nature, and will be applicable to any emerging nano technology, such as QCA, nano-CMOS designs, which may be susceptible to single or multiple transient and permanent faults.
References:


