Design and Analysis of Dual Edge Triggered Sense Amplifier Flip-Flops for Low Power Systems

Abstract: The power consumption and delay are one of the serious limitations in the low power design. The low power design used in handheld devices and also in high performance applications. As the complication increases day by day the power consumption plays an important role in the design. In recent years the requirements for high speed digital design circuits at low power applications. The flip flops are timing elements in digital circuit to determine the performance of speed and power consumption in synchronous circuits. In the research of low power VLSI circuit, the use of the dual edge triggered flip-flop has achieved more attention at the gate level design. The merit of the dual edge triggered flip-flop is to maintain a sustained output while operating at half the clock frequency. In this paper forced stack modified dual edge design technique sense amplifier flip flop is designed for low power systems. For FSMDETFF the power consumption, and optimal delay are figures of merit. The dual edge design techniques are used to reduce the half of the clock frequency to the single edge design techniques to maintain the constant throughput. This translates to higher performance in terms of both speed and power dissipation.
1. **Introduction:**

CMOS technology driven by Moore’s law, according to Moore’s law for every 18 months transistor sized is doubled which dominates the semiconductor industry. In the past decades, increasing the transistor density, there are 100 billions of transistors are fabricated on a chip which result in power consumption constantly increasing the power consumption of the VLSI chip is still increasing continuously even though the capacitances voltage scaling down is present[1]. Reducing the power dissipation of design which directly increasing the battery life of the device [21], this leads to increasing the increased power budget and complexity design. The power consumption has one of the important limitations in high performance digital designs. Power minimization technique applies to different levels of systems to minimize the power dissipation of digital system the low power techniques are applied throughout the design process the low power design used in small applications such as hand held devices. The size and weight of the device determine the amount of power required. Low power design is dealing with power minimization, power estimation and its analysis. There have been many ways of reducing power consumption in SoC (silicon on chip). The clock gating approach is widely used method for intermittently shutting down the portion of SoC. When these functional blocks are not required to be in use, another approaches for reducing power consumption DVS (dynamic voltage scaling) this can reduce the operating voltage of the entire design. This is the successful approach, but it’s limited by scalability issues. Another method to reduce the clock related power dual edge design technique instead of single edge design technique. Dual edge design can achieve same data throughput at half of the clock related power as compared to single edge design. This method does not depend on technology scaling. Power dissipation in synchronous VLSI can be divided into three major factors.

i. Power consumption in flip flop

ii. Power consumption in clock buffers

iii. Power consumption in clock network

Simple analysis shows that half of the clock frequency is to reduce the clock related power, hence the total power consumption reduced by the original design. This method can capture the data at both positive and negative edge of the clock. A challenge of dual edge design technique is to minimize the delay degradation at the half of the clock frequency. In the
single edge design technique flip-flop the output will follow input D at the edge of the clock. The difference is that the dual edge design technique flip-flop will transition on both positive and negative edge of the clock pulse on the rising and falling edge of the clock the output can change only at the clock edge the input changes the output will not be affected.

The use of the dual edge design technique used to reduce the clock frequency to the half of the single edge design while maintaining the similar data throughput [3].

2. Low Power Design:

There are 4 sources of power dissipation in CMOS circuit technology. Switching power, Short circuit power, Leakage power, Static power

\[
P_{\text{avg}} = P_{\text{switching}} + P_{\text{short-circuit}} + P_{\text{leakage}} + P_{\text{static}}
\]

\[
= \alpha C_L V_{dd} f_{ck} + I_{sc} V_{dd} + I_{\text{leakage}} V_{dd} + I_{\text{static}} V_{dd}
\]

P_{\text{switching}} is switching power. \( \alpha \) denotes the transition activity factor, i.e., the average number of power consuming transition. \( V_s \) is the voltage swing, it’s the same as the supply voltage. \( C_L \) – load capacitance. Divides into three components, gate capacitances, diffusion capacitances and interconnection capacitances.

P_{\text{short-circuit}} is short circuit power, is much smaller than the \( P_{\text{switching}} \), \( I_{sc} \) is a direct path short circuit current, it’s a path conducting from the power supply to ground from both NMOS and PMOS simultaneously on during switching.

P_{\text{leakage}} is the leakage power is determined by the fabrication technology, it has 2 sources, Reverse leakage current during parasitic drain source substrate diodes. It’s in the order of few Femto amperes which translates few micro watts of power for million transistors. The second source is sub threshold leakage current, it’s in the order of few Nano amperes, which translates into few mill watts of power for a million transistors. \( I_{\text{leakage}} \) is the leakage current.

P_{\text{static}} is a static power, \( I_{\text{static}} \) is static current appears from a circuit that have a constant current between the bias circuit and power supply. Energy is not depends on clock frequency,
battery life is determined by the amount of energy consumption. The heat dissipation is related to power consumption.

3. Review Of Existing Dual Edge Triggered Flip-Flops:

3.1. Static Output Controlled Discharged Flip-Flop (SCDFF):

It involves the explicit power generator that captures pulse data [8]. The pulse generator of the schematic is shown in fig 1, the latch structure shown in figure 2. The latch captures the pulse signal from the pulse generator. The pre-charge transistors derived from the input D. So the X follows the input D during the sampling period. The control discharge technique is to prevent the unnecessary discharge at node X.

![Figure 1: dual pulse generator](image)

The advantage of SCDFF is soft edge property low power consumption due to single end nature, the delay is always present at the output [8].

![Figure 2: LATCH](image)
3.2. Dual Edge Triggered Static Pulsed Flip-Flop (DSPFF):

![Diagram of Dual Edge Triggered Static Pulsed Flip-Flop](image)

**Figure 3: Dual edge triggered static pulsed generator**

The pulse generator of DSPFF [14] is shown in fig 3. In this four inverters are used to produce the delay clock signal and N1 and N2 is to produce the narrow sampling signal at rising and falling edge of the clock. After generating the sampling pulse the two NMOS N1 and N2 turned ON at that time the input capture by the latch so the node RB and SB discharge or charge is determined by the input data.

The D and D bar provides the signal RB and SB at the time small delay obtained. P1, P2 transfer the VDD to RB and SB and N3, N4 transfers, ground to RB and SB, respectively, if they are ON P1, P2, N1, N2 is to avoid the floating point of the node RB and SB.

![Diagram of Static Latch](image)

**Figure 4: Static Latch**

Now to analyze the disadvantage of DSPFF because of capacitive load RB and SB are extreme large, so the latency may be degraded. The high voltage drop across the transistor N3 either N4 are OFF and it suffers from high leakage current.
3.3. Adaptive Clocking Edge Sense Amplifier Flip-Flops (ACSAFF):

It consists of 3 stages adaptive clock inverting stage, sensing stage and Nikolic’s latch [7]. It’s in adaptive clocking inverter chain is disable some transistor in the chain in the switching is low in the inverter chain circuit the node NC in sensing stage to generate adaptive clocking when the input and output data are same, NC becomes too be low voltage and turn OFF the N1 and N2 transistors and it will produce the pulse.

![Figure 5: adaptive clocking inverter chain](image)

![Figure 6: sensing stage](image)

According to the sensing stage the clock signal is given to the N1,N2,N3,N4 transistors, the input D are applied to the N7 transistor and the inverted input DB is applied to N8 transistor. P1 and P2 act as load and the SB and RB are connected to Nikolic’s latch shown in figure 7. Based on the SB and RB signal the output Q and QB are generated.
The disadvantage of adaptive clocking dual edge sense amplifier flip-flops it requires number of transistors to produce the adaptive clocking and very complex circuit, in the speed will be slower and the switching activity is high, hence it will consume Lot of power due to the number of transistors used in the circuit.

3.4. Dual Edge Triggered Sense Amplifier Flip-Flop (DETFF):

The schematic of dual pulse generator[28] shown in figure 8: the clock is applied, i.e. the rising edge of the clock(+ve edge) the clock1 is LOW, clock2 is HIGH and clock3 is LOW, at that time N2 is OFF and P1 is LOW, the clock is HIGH the N1 is ON and to produce a short output pulse. When the clock is LOW, the P1 gets ON and N1 gets off, the clock2 is LOW the P2 is ON and clock 3 is LOW, N3 is OFF at the time a small output pulse is generated. Hence very short pulses are generated at the both positive and negative edge of the clock.
Sense amplifier [28] is used to reduce the signal propagation, it’s an active circuit and the arbitrary logic is converted into digital logic. The D input is applied to P1 and DB is applied to N1. The output of pulses generated signal is applied to N2 and P2 of sense amplifier circuit in the evaluation phase the D is set to low the RB will be and SB also high. The precharge technique is applied to DETFF is to avoid the redundant transition, if the D is set to high the SB will get discharged. When the pulse is low SB will float DB is high, RB is precharged this reduce the discharging time significantly. Sensing stage is used to reduce the low power and for high speed.

Further to increase the flip-flop speed performance the latch is proposed. The latch circuit is shown in figure 10. Based on the sensing stage SB and RB are operated to the latching stage transistor P4 and N2 act as inverter and P8 and N4 form a another inverter structure. Due to single ended nature the delay is always present at the output. So the power dissipation exists.
4. Proposed Techniques:

4.1. Modified Dual Edge Triggered Sense Amplifier Flip-Flop (MDETFF):

The pulse generator of modified dual edge triggered sense amplifier flip-flop shown in figure 12. In this circuit, we reduced the number of inverters when compared to the dual edge triggered flip-flop. When the a clock is HIGH NMOS N1 gets turned ON and P1 PMOS OFF and I1 is LOW so N2 is OFF, I2 is HIGH the P2 remains OFF at that time short time pulse is obtained. When the CLOCK was LOW at that time PMOS P1 is ON and N1 is OFF, I1 is HIGH, N2 ON, I2 was LOW at that time a short time pulse obtained.

Sense amplifier is used to reduce the signal propagation, it’s an active circuit and the arbitrary logic is converted into digital logic. The D input is applied to P1 and DB is applied to N1. The output of pulses generated signal is applied to N2 and P2 of sense amplifier circuit in the evaluation phase the D is set to low the RB will be and SB also high. The precharge technique is applied to DETFF is to avoid the redundant transition, if the D is set to high the SB will get discharged. When the pulse is low SB will float DB is high, RB is precharged this reduce the discharging time significantly. Sensing stage is used to reduce the low power and for high speed.
Further to increase the flip-flop speed performance the latch is proposed. The latch circuit is shown in figure 13. Based on the sensing stage SB and RB are operated to the latching stage transistor P4 and N2 act as inverter and P8 and N4 form a another inverter structure. Due to single ended nature the delay is always present at the output. So the power dissipation exists. Advantage of modified dual edge triggered sense amplifier flip-flop, we are reducing the number of transistors in pulse generator circuit so the circuit is very simplex to generate a narrow pulse at both positive and negative edge of the clock. So the speed of the flip-flop is higher, hence the switching activity is reduced, hence the power consumption reduced.

4.2. Forced Stack Dual edge Triggered Flip-Flop (FSDETFF):

Figure 14: forced stack pulse generator
The forced stack dual edge pulse generator is shown in figure14. P2, N3, N4 are the force stacking transistor are helps to reduce the leakage power when compare to single OFF device. In this four inverters are used to produce the delay clock signal and N1 and N2 is to produce the narrow sampling signal at only falling edge of the clock. After generating the sampling pulse the two NMOS N1 and N2 turned ON at that time the input capture by the latch so the node RB and SB discharge or charge is determined by the input data. The D and D bar provides the signal RB and SB at the time small delay obtained. P1, P2 transfer the VDD to RB and SB and N3, N4 transfers, ground to RB and SB, respectively, if they are ON P1, P2, N1, N2 is to avoid the floating point of the node RB and SB. Now to analyze the disadvantage of DSPFF because of capacitive load RB and SB are extreme large, so the latency may be degraded. The high voltage drop across the transistor N3 either N4 are OFF and it suffers from high leakage current.

Figure 15: sensing stage

Sense amplifier is used to reduce the signal propagation, it’s an active circuit and the arbitrary logic is converted into digital logic. The D input is applied to P1 and DB is applied to N1. The output of pulses generated signal is applied to N2 and P2 of sense amplifier circuit in the evaluation phase the D is set to low the RB will be and SB also high. The precharge technique is applied to DETFF is to avoid the redundant transition, if the D is set to high the SB will get discharged. When the pulse is low SB will float DB is high, RB is precharged this reduce the discharging time significantly. Sensing stage is used to reduce the low power and for high speed.
After generating the sampling pulse the 2 NMOS N1 and N2 turned ON based on the sensing signal, the SB connected to P0 and RB connected to N5. The node A and B are charged/discharge determined by input data. The P0 and N5 transistor are helps to reduce the leakage power so power dissipation is less when compare to MDETFF. Even though the P0 and N5 transistor reduce the leakage power the power consumption is linearly increases for various load capacitances.

4.3. Forced Stack Modified Dual Edge Triggered Flip-Flop (FSMDETFF):

The forced stack dual edge pulse generator are shown in figure 17. P2, N3, N4 are the force stacking transistor are helps to reduce the leakage power when compare to single OFF device. The drive current of forced stack gate is lower, and increasing delay, it’s is used only the path are not critical. In this technique the path are faster and hence saving the leakage it’s also can reduce the standby and active leakage of non-critical path. Either P1, P2 or N3,N4 transistor turns OFF then stacking effect reduces the subthreshold leakage current. All the four transistor N3,N4,P1,P2 are getting same clock input so these force stack technique is a stack saving technique. When the circuit is OFF mode it save the current state.
In this four inverters are used to produce the delay clock signal and N1 and N2 is to produce the narrow sampling signal at only falling edge of the clock. Latch has been discussed in section

![Figure 18: sensing stage](image)

Sense amplifier is used to reduce the signal propagation, it’s an active circuit and the arbitrary logic is converted into digital logic. The D input is applied to P1 and DB is applied to N1. The output of pulses generated signal is applied to N2 and P2 of sense amplifier circuit in the evaluation phase the D is set to low the RB will be and SB also high. The precharge technique is applied to DETFF is to avoid the redundant transition, if the D is set to high the SB will get discharged. When the pulse is low SB will float DB is high, RB is precharged this reduce the discharging time significantly. Sensing stage is used to reduce the low power and for high speed.

![Figure 19: latching stage](image)

Latch circuit are already discussed in section 2. The force stack modified dual edge triggered flip-flop is consume less power compare to other dual edge design techniques.
5. Simulation Setup:

![Simulation Setup Flow Chart](image.png)

*Figure 20: simulation setup flow chart*

For the simulation we used two types of softwares namely DSCH/microwind. DSCH is Digital Schematic Editor and Simulator used to analyze the circuits input, output characteristics and it generates the Verilog file.

Microwind is used for layout design, which is used to extract the layout from DSCH generated Verilog file, hence to analyze the various parameters like load capacitances, temperature and temperature.

6. Simulation Result:

<table>
<thead>
<tr>
<th>DUAL EDGE DESIGN TECH</th>
<th>POWER DISSIPATION IN MILLIWATTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCDFF</td>
<td>0.390</td>
</tr>
<tr>
<td>DSPFF</td>
<td>0.026</td>
</tr>
<tr>
<td>ACSAFF</td>
<td>0.167</td>
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<tr>
<td>DETFF</td>
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<tr>
<td>MDETFF</td>
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<tr>
<td>FSDETFF</td>
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<tr>
<td>FSMDETFF</td>
<td>0.010</td>
</tr>
</tbody>
</table>

*Table 1: Power dissipation factor*
In the table 1 shows that the power dissipation for various dual edge design techniques in that the FSMDETFF consumes less power when compare to other dual edge design techniques.

![Power Dissipation Graph for Dual Edge Designs](image1)

*Figure 21: Power dissipation graph for dual edge designs*

In the fig 21 represent the power dissipation graph for various dual edge design techniques and the table 2 shows that the power dissipation for various capacitance. The FSMDETFF and MEDETFF have produced the constant value for various capacitances. And increasing the circuit robustness the fig 22 represent the graph for various capacitances.

![Power Dissipation for Various Capacitances](image2)

*Figure 22: Power dissipation for various capacitances*
Figure 23: power dissipation for various Vdd

Figure 24: power dissipation for various temperature
<table>
<thead>
<tr>
<th>POWER DISSIPATION FOR LOAD CAPACITANCES</th>
<th>DUAL EDGE DESIGN TECHNIQUES</th>
<th>VDD IN volts</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SCDFF</td>
<td>DSPFF</td>
</tr>
<tr>
<td>0</td>
<td>0.390</td>
<td>0.026</td>
</tr>
<tr>
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<tr>
<td>20</td>
<td>0.384</td>
<td>0.032</td>
</tr>
<tr>
<td>30</td>
<td>0.384</td>
<td>0.034</td>
</tr>
<tr>
<td>40</td>
<td>0.384</td>
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<tr>
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<tr>
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<td>0.384</td>
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<tr>
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<td>0.049</td>
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<tr>
<td>90</td>
<td>0.383</td>
<td>0.052</td>
</tr>
<tr>
<td>100</td>
<td>0.383</td>
<td>0.054</td>
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Table 2: power dissipation for various capacitances

<table>
<thead>
<tr>
<th>POWER DISSIPATION FOR TEMPERATURE</th>
<th>SCDFF</th>
<th>DSPFF</th>
<th>ACSAFF</th>
<th>DETFF</th>
<th>MDETFF</th>
<th>FSDETFF</th>
<th>FSMDETFF</th>
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<tr>
<td>-40</td>
<td>0.397</td>
<td>0.024</td>
<td>0.129</td>
<td>0.022</td>
<td>0.018</td>
<td>0.01</td>
<td>0.01</td>
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<tr>
<td>-20</td>
<td>0.384</td>
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<td>0.019</td>
<td>0.011</td>
<td>0.01</td>
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<tr>
<td>0</td>
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<tr>
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<td>0.019</td>
<td>0.018</td>
<td>0.011</td>
</tr>
<tr>
<td>40</td>
<td>0.411</td>
<td>0.03</td>
<td>0.17</td>
<td>0.024</td>
<td>0.02</td>
<td>0.022</td>
<td>0.011</td>
</tr>
<tr>
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<td>0.432</td>
<td>0.032</td>
<td>0.17</td>
<td>0.024</td>
<td>0.02</td>
<td>0.027</td>
<td>0.011</td>
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<tr>
<td>80</td>
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<td>0.172</td>
<td>0.026</td>
<td>0.021</td>
<td>0.033</td>
<td>0.011</td>
</tr>
</tbody>
</table>

Table 4: power dissipation for various Temperature
7. Conclusion:

In this thesis the 3 techniques are designed, modified dual edge triggered flip-flop are help to reduce the number of transistors in pulse generator circuit, so the area is reduced and power dissipation also reduced. Then to further reduce the power dissipation we designed force stack dual edge triggered flip-flop. The FSDETFF is help to reduce the leakage current when compare to single off device. In this FSDETFF the latch circuit are designed in that P0 and N5 are used to reduce the leakage current, hence it consume less power when compare to MDETFF, but it linearly increase in power dissipation when changes occurs in load capacitances. So to avoid this we finally designed the forced stack modified dual edge triggered flip-flop, the FSMDETFF is helps to reduce the leakage current so the power dissipation also reduced and also it helps to improve the circuit robustness. In this FSMSETFF that the path are faster and hence saving the leakage and also reduce the sub-threshold voltage when the two or more transistors turned OFF. The FSMDETFF are save more power when compare to other dual edge design techniques, which translate to better performance in-terms of both speed and power.
References:


